intellux
INCORPORATED

HYBRID MICROCIRCUIT PERFORMANCE CHARACTERISTICS

SPECIFICATION
NOR/NAND GATES
SERIES M
DATA

INTELLUX INCORPORATED, SANTA BARBARA RESEARCH PARK, 26 COROMAR DRIVE, GOLETA, CALIFORNIA, PHONE (805) 968-3541, CABLE: INTLUX

Intellux NOR/NAND gate hybrid microcircuits make optimum use of the design simplicity, inherent stability, and excellent noise immunity of saturated transistor logic. Silicon planar epitaxial transistors are used throughout. The circuits are offered in RTL (medium frequency) and RCTL (high frequency) designs.

When used in positive-logic (binary "1" more positive than binary "0") systems, they perform as NOR gates or the De Morgan AND gate complement:

When used in negative-logic (binary "0" more positive than binary "1") systems, they perform as NAND gates or the De Morgan OR gate complement:

The following circuit types are described in this bulletin:

1. Dual 3-Input NOR/NAND Gate
2. 5-Input NOR/NAND Gate
3. 3-Input Buffered NOR/NAND Gate
4. 3-Input NOR/NAND Gate and Buffer

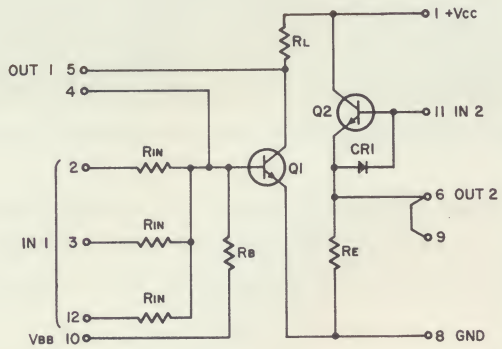
TYPE DESIGNATIONS

NOR/NAND GATE TYPES	R T L			R C T L		
	Sch. No.	1/2 Std. Ω/□	Std. Ω/□	Sch. No.	1/2 Std. Ω/□	Std. Ω/□
Dual 3-Input NOR/NAND Gate	50	GG14□4B	GG15□4B	150	GG34□5C	GG35□5C
5-Input NOR/NAND Gate	60	GG24□4B	GG25□4B	160	GG44□5C	GG45□5C
3-Input Buffered NOR/NAND Gate	10	GB14□4B	GB15□4B	110	GB24□5C	GB25□5C
3-Input NOR/NAND Gate and Buffer	11	GB14□4G	GB15□4G	111	GB24□5H	GB25□5H

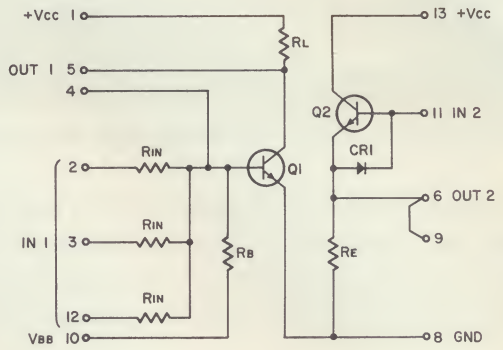
□ Note: Blank square in type numbers reserved for profile designator; Number 1 indicates Standard Profile, Number 2 indicates Low Profile. Example:
GG1514B = Dual 3-Input NOR/NAND Gate; Standard Profile
GG1524B = Dual 3-Input NOR/NAND Gate; Low Profile

Bulletin No. SD-08-66

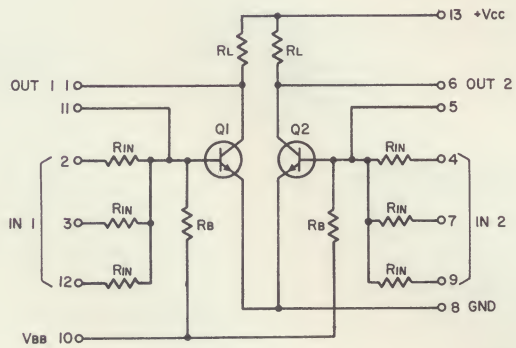
SCHEMATIC DIAGRAMS
RTL (MF) NOR/NAND GATES



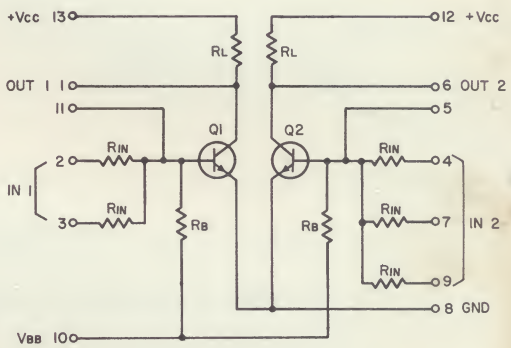
SCH. 10 3-INPUT BUFFERED NOR/NAND GATE



SCH. 11 3-INPUT NOR/NAND GATE AND BUFFER

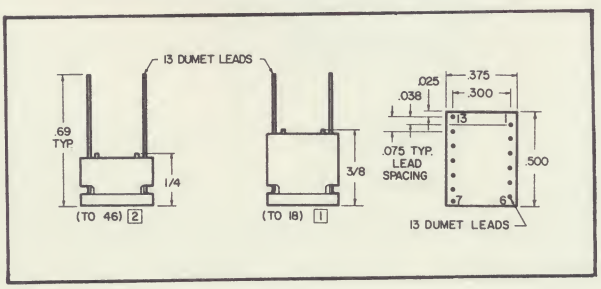


SCH. 50 DUAL 3-INPUT NOR/NAND GATE

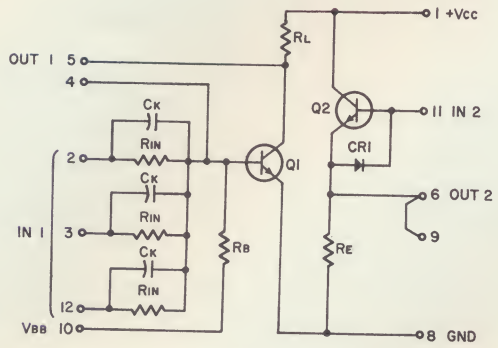


SCH. 60 5-INPUT NOR/NAND GATE

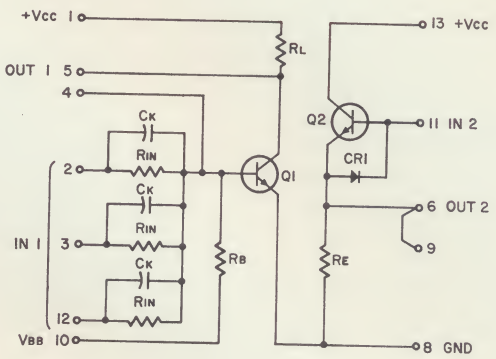
INSTALLATION DIAGRAM



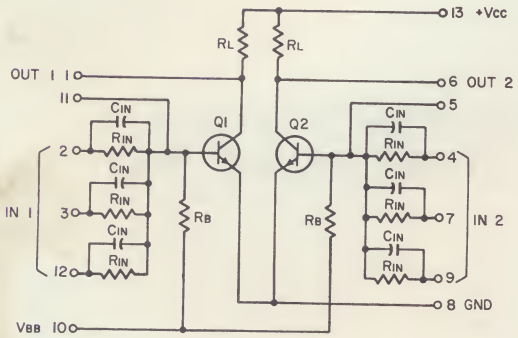
SCHEMATIC DIAGRAMS
RCTL (HF) NOR/NAND GATES



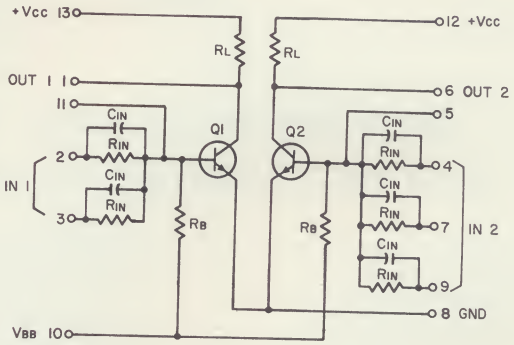
SCH. 110 3-INPUT BUFFERED NOR/NAND GATE



SCH. 111 3-INPUT NOR/NAND GATE AND BUFFER



SCH. 150 DUAL 3-INPUT NOR/NAND GATE



SCH. 160 5-INPUT NOR/NAND GATE

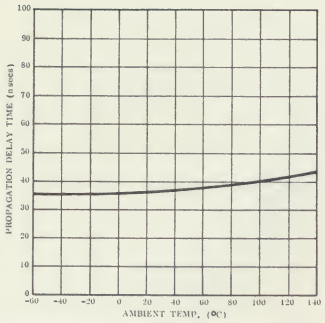
COMPONENTS

Q 1,2: 2N2369A SERIES
CRI: IN914 SERIES

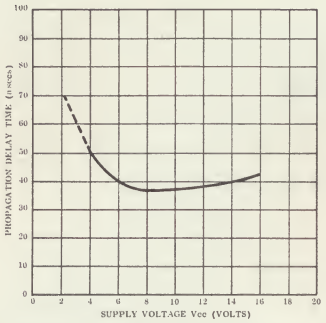
	RB	RIN	RE, RL
1/2 STD Ω/□	12.6K	3.4K	.75K
STD Ω/□	25.2K	6.8K	1.5K

CK = 7pF CIN = 7pF

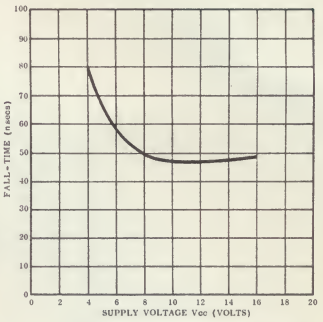
RTL(MF) NOR/NAND GATES PERFORMANCE CHARACTERISTICS @ 1 MHz (TYPE GG 15☐4B)



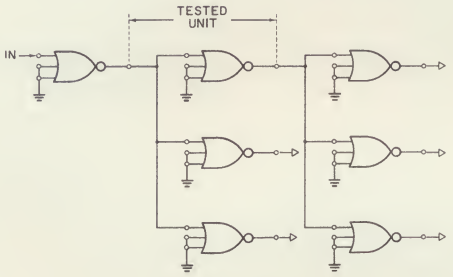
TYPICAL PROPAGATION DELAY TIME PER STAGE vs AMBIENT TEMP. SUPPLY VOLTAGE Vcc = 9.0V



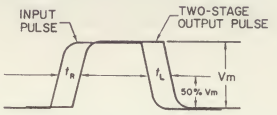
TYPICAL PROPAGATION DELAY TIME PER STAGE vs SUPPLY VOLTAGE (25°C AMBIENT TEMP.)



TYPICAL OUTPUT PULSE FALL-TIME vs SUPPLY VOLTAGE (25°C AMBIENT TEMP.)



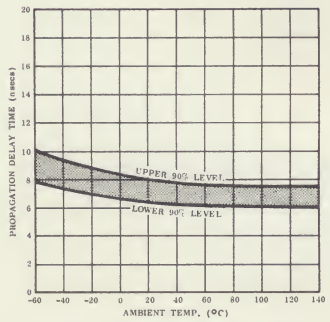
CIRCUIT A



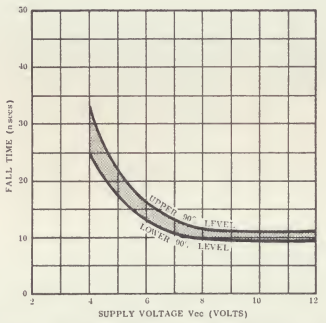
AVERAGE PROPAGATION DELAY TIME (per stage)

$$t_{av} = \frac{t_L + t_R}{4}$$

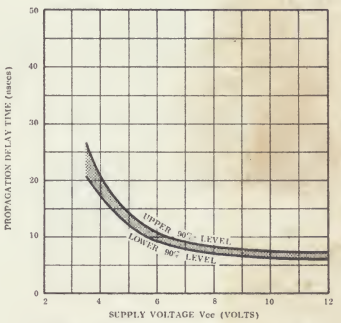
RCTL(HF) NOR/NAND GATES PERFORMANCE CHARACTERISTICS @ 1 MHz (TYPE GG 34☐5C)



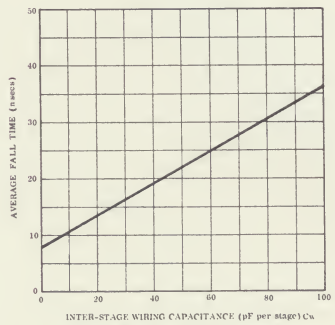
PROPAGATION DELAY TIME vs AMBIENT TEMP. (Vcc = 8.5V, Cw = 10pF / stage)



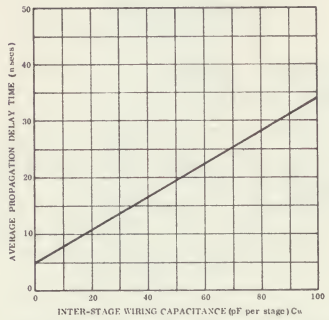
FALL TIME vs SUPPLY VOLTAGE (T_{AMB} = 25°C, Cw = 10pF / stage)



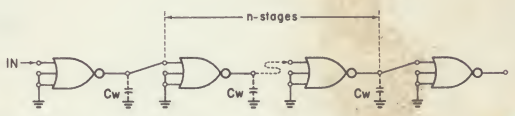
PROPAGATION DELAY TIME vs SUPPLY VOLTAGE (T_{AMB} = 25°C, Cw = 10pF / stage)



AVERAGE FALL TIME vs WIRING CAPACITANCE (T_{AMB} = 25°C, Vcc = 8.5V)



AVERAGE PROPAGATION DELAY TIME vs WIRING CAPACITANCE (T_{AMB} = 25°C, Vcc = 8.5V)



AVERAGE PROPAGATION DELAY TIME (per stage)

$$t_{av} = \frac{t_L + t_R}{2n}$$

CIRCUIT B

Cw – distributed inter-stage wiring capacitance

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LINIPAK

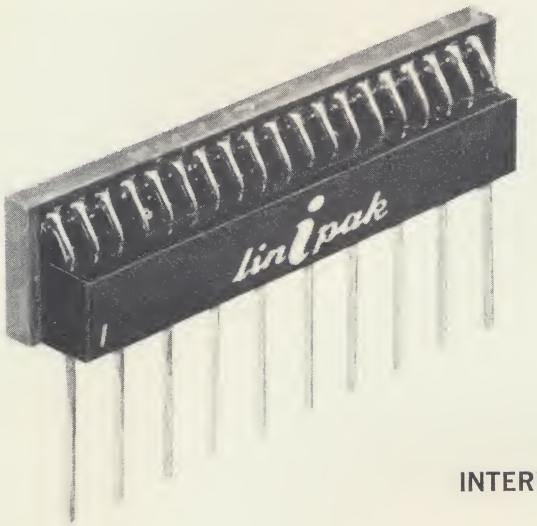
PRICING

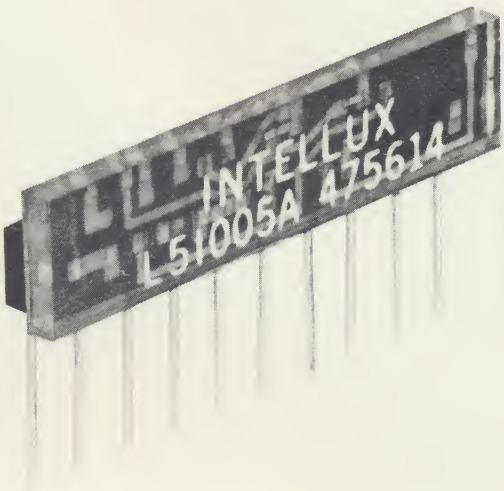
SERIES LB

DATA

INTELLUX INCORPORATED, SANTA BARBARA RESEARCH PARK, 26 COROMAR DRIVE, GOLETA, CALIFORNIA, PHONE (805) 968-3541, CABLE: INTLUX

AUGUST 1966





INTERFACE DRIVERS

	1 - 25	26 - 50	51 - 100	101 - 500	501 - 1000
L-51003	8.25	7.20	6.10	5.55	5.00
L-51010	8.10	7.05	5.90	5.45	4.90
L-51015	8.10	7.05	5.90	5.45	4.90

ORDERING DATA

DELIVERY: Stock or twenty days

TERMS: Net 30 days

F.O.B. POINT: Goleta, California 93017

MIXED LOT: Special pricing for mixed lots of 501 and up

VOLUME PRICING: Available from manufacturer upon request

BULLETIN NO. LB-P-866

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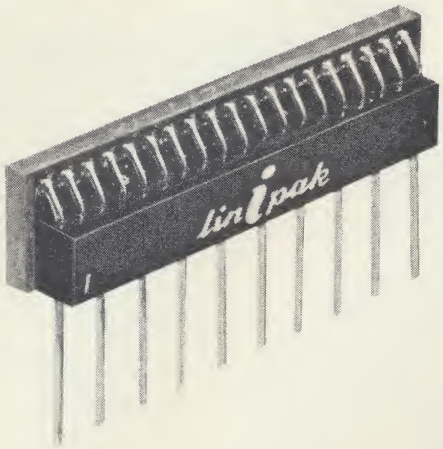
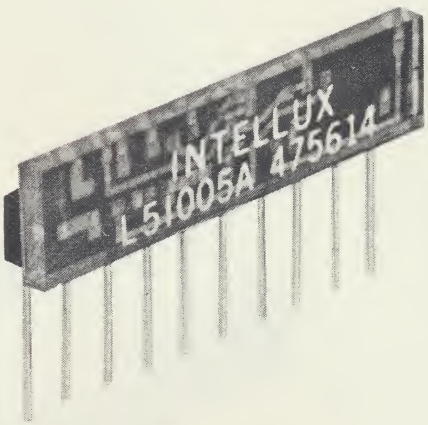
LOGIC-AL APPLICATIONS OF HYBRID MICROCIRCUITS

INTELLOGIC
linipak
BULLETIN

INTELLUX INCORPORATED, SANTA BARBARA RESEARCH PARK, 26 COROMAR DRIVE, GOLETA, CALIFORNIA, PHONE (805) 968-3541, CABLE: INTLUX





LINIPAK™ — A NEW CONCEPT IN HYBRID MICROCIRCUITS

LINIPAK,™ a unique and practical approach to hybrid microcircuitry, is the result of a new packaging concept developed by Intellux, Inc. Based on an assembly process comparable to the technique employed by a linotype machine in contemporary printing practice, thin film passive networks are combined with flat discrete active components to provide compact, reliable microcircuits at minimum cost. Significant advantages are offered in both commercial and industrial usage for digital, linear, and custom interface applications. The prime features of the LINIPAK™ method are:

- "In-line" construction which results in a unique thin-form circuit envelope. Savings to 50% in printed circuit board area over the standard dual in-line construction are realized.

- A high ratio of active/passive elements provides for a high degree of design flexibility.

- Relatively complex microcircuits can be produced quickly and inexpensively to exact customer specifications. Hybrid circuit assembly costs and rejects are drastically reduced through employment of fully pretested geometrically compatible semiconductor and passive network components.

- The package form allows for complete visual inspection of all connections to the thin-film microcircuit.

Bulletin No. LI-18-66

PACKAGE CONSTRUCTION

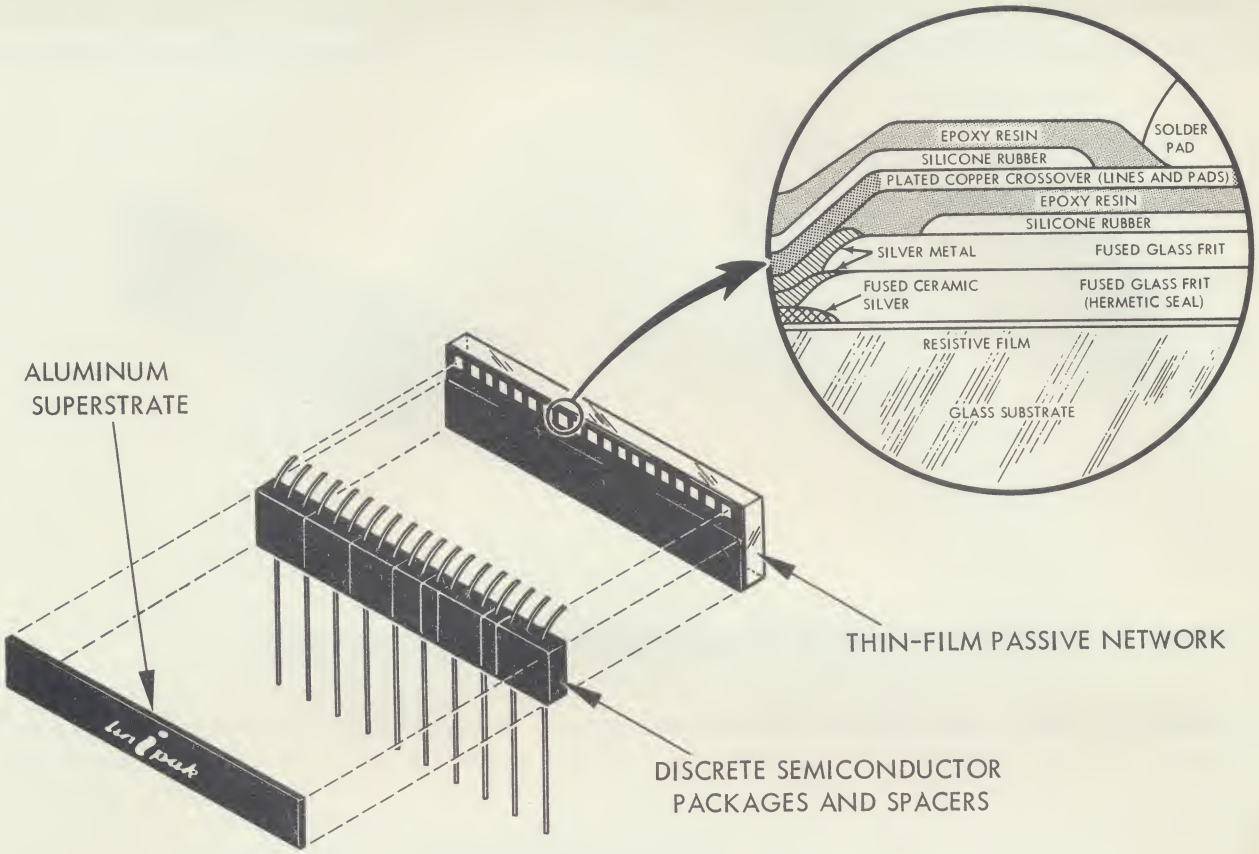


Figure 1. Exploded View of LINIPAK™ Package. Insert illustrates cross-section of a typical Intellux thin-film passive circuit.

As illustrated by Figure 1, LINIPAK™ thin-form construction consists of:

(1) A glass substrate with deposited thin-film tin-oxide resistors, glass dielectric capacitors, and integral interconnections.

(2) Flat, three-lead plastic semiconductor packages.

(3) Single, double, or triple-lead spacers.

(4) An aluminum superstrate to dissipate heat and serve as a mechanical stiffener.

Leads from one edge of the semiconductors and spacers are wave-soldered to the thin-film substrate connection pads; selected leads from the opposite edge form the connecting leads of the device. All unused connecting leads are trimmed off after assembly, giving lead spacing distances of 100 mils or more in increments of 50 mils. This feature will allow the punching (instead of drilling) of mounting holes in printed circuit cards used with LINIPAK™ units. A further advantage inherent in this packaging technique is the use of rectilinear inter-connections between units without pin interferences.

The heart of the LINIPAK™ circuit is the passive network which is manufactured in accordance with proven thin-film techniques (see insert, Figure 1). Passive components are deposited on the surface of a glass substrate of high volume resistivity. Negligible ionic migration in this glass prevents electrolytic corrosion of the subsequently applied resistive film. The glass has many physical and chemical properties particularly suited to subsequent processing and ultimate utilization. For example, the expansivity of 5.2 ppm/^{o}C is very close to the expansivity of tin oxide, the resistive film material. This close match results in greater resistor stability.

The resistive film is applied by uniform pyrolytic deposition. Film thicknesses are typically 2500 Å. The resistor configuration and termination areas are photo-etched with minimum line widths (for conservative design) standardized at 0.003". Fired-on silver terminations and capacitor plates are applied by silk screening and the film is hermetically sealed by applying fuseable powdered glass insulations selectively over the film areas and capacitor plates. The same fused glass films also serve as the dielectric material for capacitors. A suitable upper interconnection pattern is electro-plated and photo-etched after the components are subjected to a stabilization procedure.

Resistor values with optimized properties are developed at approximately four megohms per square inch (80 ohms per square); capacitors at 3500 picofarads per square inch. Standard film resistivities range from 20 - 500 ohms per square.

Intellux thin-film microcircuits are both extremely stable and reliable because:

(1) The resistive film and fused dielectrics are capable of withstanding temperatures to 500^{o}C without significant degradation.

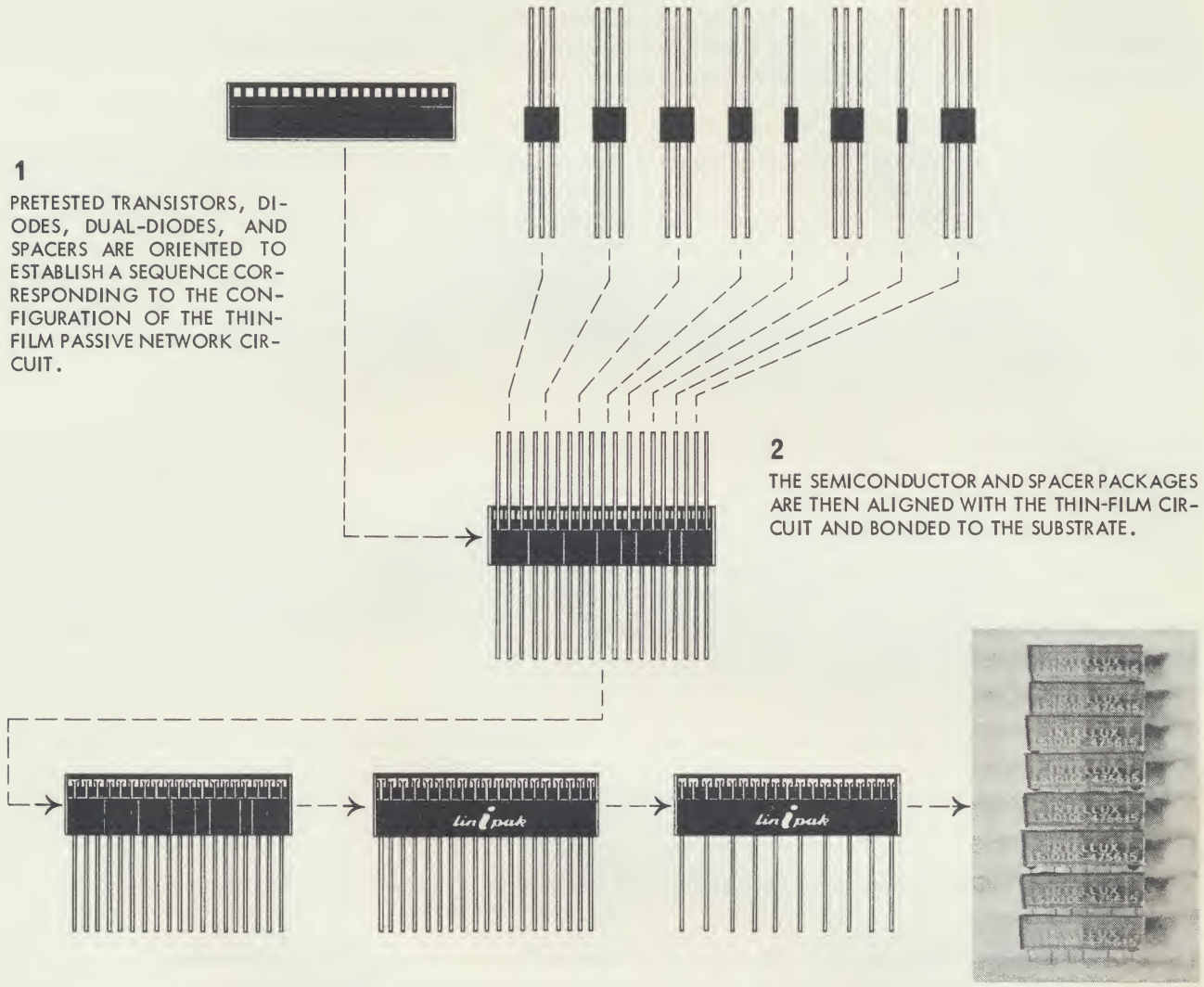
(2) The glass superstrate protects the film from the environment.

(3) The product is operated at temperatures well below its inherent limitations.

FABRICATION TECHNIQUE

LINIPAK™ design is particularly suited for fully automated production as illustrated by the assembly sequence shown below. As indicated previously, the assembly process is compa-

rable to the technique employed by a linotype machine in contemporary printing practice.



1

PRETESTED TRANSISTORS, DIODES, DUAL-DIODES, AND SPACERS ARE ORIENTED TO ESTABLISH A SEQUENCE CORRESPONDING TO THE CONFIGURATION OF THE THIN-FILM PASSIVE NETWORK CIRCUIT.

2

THE SEMICONDUCTOR AND SPACER PACKAGES ARE THEN ALIGNED WITH THE THIN-FILM CIRCUIT AND BONDED TO THE SUBSTRATE.

3

LEADS FROM THE SEMICONDUCTORS TO THE THIN-FILM PASSIVE NETWORK ARE TRIMMED, BENT TO MEET THE SUBSTRATE CONNECTING PODS & WAVE SOLDERED.

4

AN ALUMINUM SUPERSTRATE USED FOR MECHANICAL STIFFENING & HEAT DISSIPATION IS BONDED TO THE CIRCUIT SUBASSEMBLY. EACH ASSEMBLY IS THEN SUBJECTED TO ULTRASONIC CLEANING, AND FINAL ELECTRONIC TESTING.

5

UNUSED SEMICONDUCTOR LEADS ARE CUT OFF GIVING LEAD SPACING DISTANCES OF 100 MILS OR MORE IN STEPS OF 50 MILS.

6

COMPLETED UNITS ARE PACKAGED FOR SHIPMENT.

CURRENT PRODUCTION

Currently in production is the LINIPAK™ Series LA which consists of a complete line of level transformation devices for use with emitter-coupled logic. Other interface families compatible with TTL, DTL and other monolithic integrated circuits will soon be available. In addition, Intellux, Inc. manufactures a wide variety of custom digital and analog circuits and carded systems to customer specifications.

intellux
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HYBRID MICROCIRCUIT PERFORMANCE CHARACTERISTICS

SPECIFICATION

INTERFACE DRIVERS

DATA

INTELLUX INCORPORATED, SANTA BARBARA RESEARCH PARK, 26 COROMAR DRIVE, GOLETA, CALIFORNIA, PHONE (805) 968-3541, CABLE: INTLUX

The LIN•I•PAK™ hybrid microcircuit consists of thin film passive networks which are combined with flat discrete active components to provide a compact and highly reliable hybrid at a nominal price. This technique permits —

- ☐ An "IN-LINE", thin-form circuit envelope. (Savings to 50% in printed circuit board area over dual in-line configurations.)
- ☐ High ratio of active-to-passive components for maximum design flexibility.
- ☐ Drastic reduction of complex circuit assembly costs by utilization of pre-tested, geometrically compatible, active and passive networks.

The LIN•I•PAK LB series has been specifically designed to perform the interface function of current and voltage translation necessary for proper operation of relays, lamps, and other high-load devices from low-voltage swing logic circuits such as ECL, TTL, DTL, etal. The wide range of input parameters (—0.75V to +4.5V) provides latitude for enhancing system optimization. Output parameters (+30 V, 150mA) eliminate the need for intermediate transformation.

The LB series is typical of the Intellux hybrid design in that it offers the highest possible noise immunity (3. OV typ.) together with compatible rise and fall times.

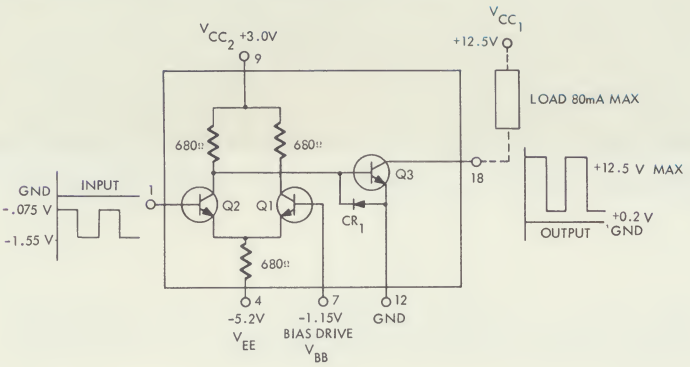
Attention is directed to the fact that with appropriate modifications this family of devices may be used to interface with many other types of loads such as telephone relays, stepping switches, stepping motors and a wide variety of optical indicators.
Please contact Intellux for further details.

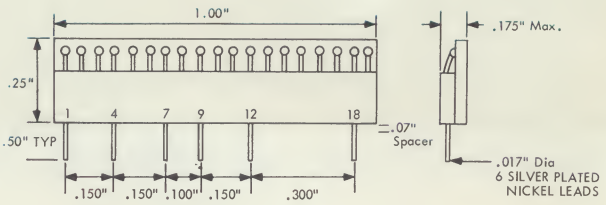
OPERATIONAL CHARACTERISTICS

PART NO.	INPUT LEVELS (VOLTS)		OUTPUT LEVELS (VOLTS)	
	"0"	"1"	"0"	"1"
L51003B	—1.55	—0.75	+0.2	+6.0 to +12.5
L51010A*	—1.55	—0.75	+0.2	+6.0 to +30.0
L51015A	+0.2	+4.5	+0.2	+6.0 to +30.0

*For Performance Details Refer to L51003B

HYBRID DRIVER — L51003B





OPERATIONAL CHARACTERISTICS

LOGIC STATE	INPUT LEVELS (VOLTS)	OUTPUT LEVELS (VOLTS)	POWER SUPPLY REQUIREMENTS (mA)				
			I_{IN}	I_{CC_1}	I_{EE}	I_{BB}	I_{CC_2}
"0"	−1.55	+0.2	0	76.5	4.6	.05	7.6
"1"	−0.75	+6.0 to +12.5	.04	0	5.2	0	5.3

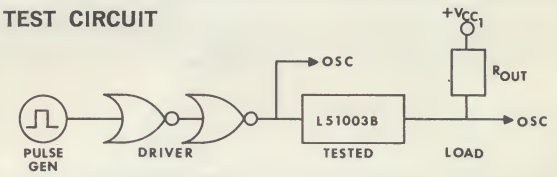
PARAMETER DERIVATION METHOD

TEST CONDITIONS

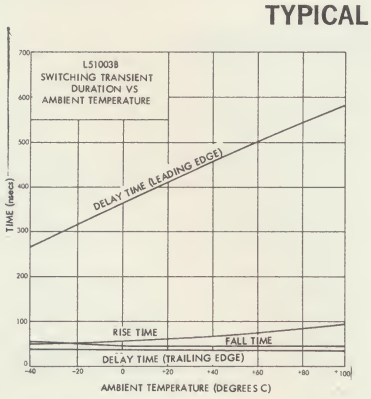
$V_{CC1} = +12.5V$ (or var)
$V_{EE} = -5.2V$
$V_{BB} = -1.15V$
$V_{CC2} = +3.0V$

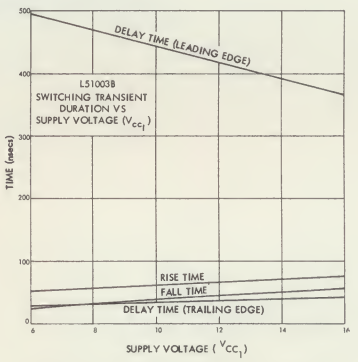
T amb = 25°C (or var)
R out = 160Ω (or var)
OSC: — Tektronix Type 585
DRIVER: MC 359 G

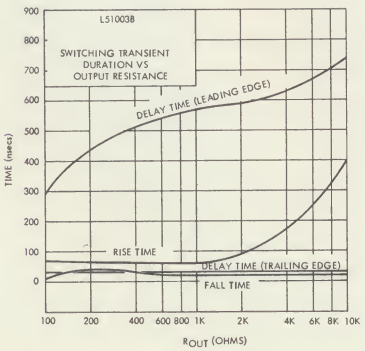
TEST CIRCUIT

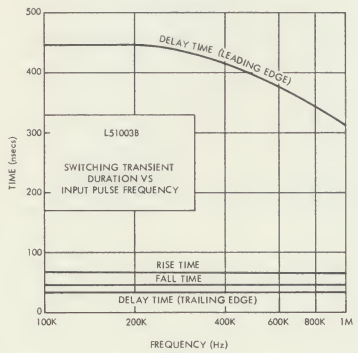


TYPICAL CHARACTERISTICS

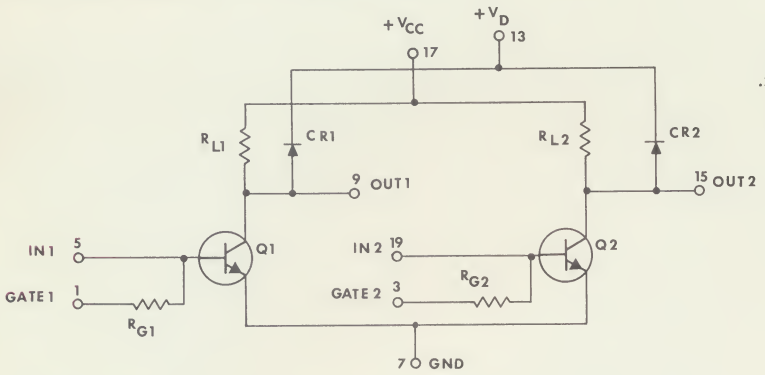


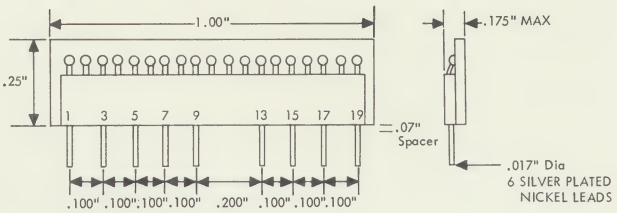






HYBRID DRIVER — L51015A





OPERATIONAL CHARACTERISTICS

LOGIC STATE	INPUT LEVELS (VOLTS)	OUTPUT LEVELS (VOLTS)	POWER SUPPLY REQUIREMENTS (mA)				
				I_{CC}	I_D	I_G	
"0"	+0.2	+0.2		0	0	−3	
"1"	+4.5	+6.0 to +30.0		4.7	25nA	−15	

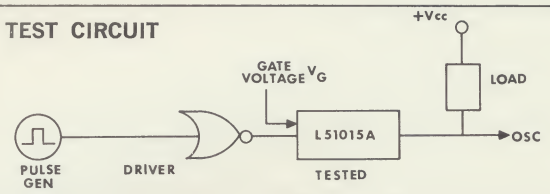
PARAMETER DERIVATION METHOD

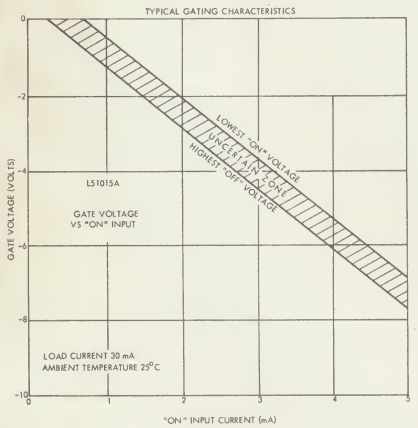
TEST CONDITIONS

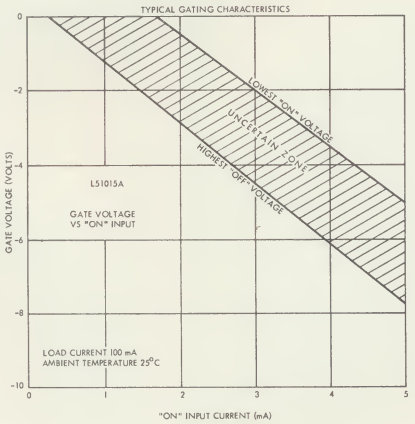
$V_{CC} = +12.0V$
$V_D = +12.0V$
V_G = Variable

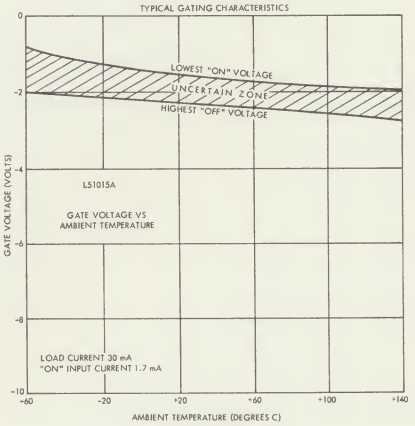
T amb = 25°C
LOAD = 140 mA (max)
OSC: Tektronix Type 585
DRIVER: Intellux GG 1514B

TEST CIRCUIT









intellux
INCORPORATED

HYBRID MICROCIRCUIT PERFORMANCE CHARACTERISTICS

SPECIFICATION

LOGIC LEVEL ADJUSTORS

DATA

INTELLUX INCORPORATED, SANTA BARBARA RESEARCH PARK, 26 COROMAR DRIVE, GOLETA, CALIFORNIA, PHONE (805) 968-3541, CABLE: INTLUX

The LIN•I•PAK™ hybrid microcircuit consists of thin film passive networks which are combined with flat discrete active components to provide a compact and highly reliable hybrid at a nominal price. This technique permits —

- ☐ An "IN-LINE", thin-form circuit envelope. (Savings to 50% in printed circuit board area over dual in-line configurations.)
- ☐ High ratio of active-to-passive components for maximum design flexibility.
- ☐ Drastic reduction of complex circuit assembly costs by utilization of pre-tested, geometrically compatible, active and passive networks.

The LIN•I•PAK LA series is a family of interface circuits which have been designed specifically for use with emitter-coupled logic (ECL). They enhance the already exceptional performance of ECL circuits by adjusting the voltage swings from typical values of —0.75 and —1.55V to levels on the order of 12 volts.

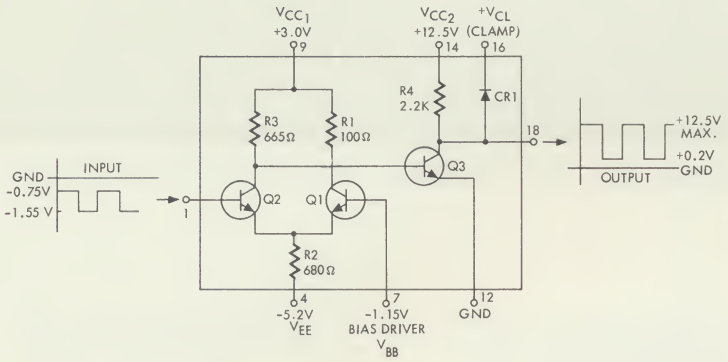
The LA series is typical of the Intellux hybrid microcircuit in that it offers the highest possible noise immunity (3.0V typ.) together with high frequency performance and compatible rise and fall times.

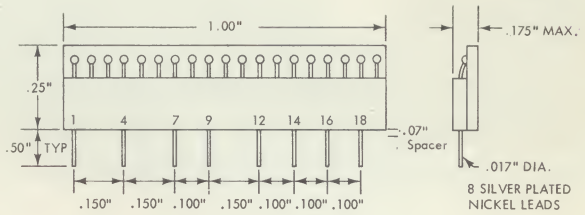
Attention is directed to the fact that, with appropriate modifications, interface with other logic schemes such as TTL, DTL, RTL, RCTL, etal is readily achievable. Please contact Intellux for further details.

OPERATIONAL CHARACTERISTICS

	INPUT LEVELS (VOLTS)		OUTPUT LEVELS (VOLTS)	
PART NO.	"0"	"1"	"0"	"1"
L51001B	—1.55	—0.75	+0.2	+6.0 to +12.5
L51002B	—1.55	—0.75	—6.0 to —12.5	—0.2
L51004A	+0.2	+6.0 to +12.5	—1.55	—0.75
L51005A	—6.0 to —12.5	—0.2	—1.55	—0.75

LEVEL ADJUSTORS — L51001B





OPERATIONAL CHARACTERISTICS

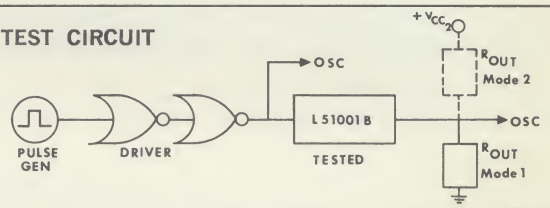
LOGIC STATE	INPUT LEVELS (VOLTS)	OUTPUT LEVELS (VOLTS)	POWER SUPPLY REQUIREMENTS (mA)				
			I_{IN}	I_{CC2}	I_{EE}	I_{BB}	I_{CC1}
"0"	−1.55	+0.2	0	5.4	4.6	.05	7.6
"1"	−0.75	+6.0 to +12.5	.04	0	5.2	0	5.3

PARAMETER DERIVATION METHOD

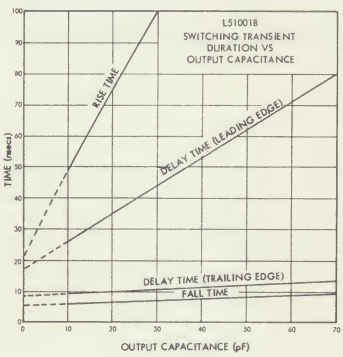
TEST CONDITIONS

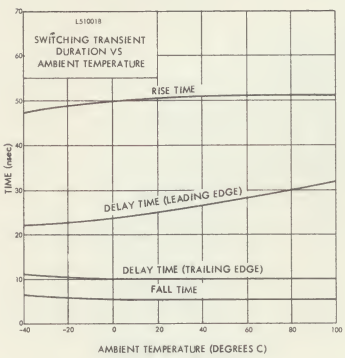
$V_{CC2} = +12.5V$ (or var)
$V_{EE} = -5.2V$
$V_{BB} = -1.15V$
$V_{CC1} = +3.0V$
T amb = 25°C (or var)
R out = 2.2K (Mode 1)
R out = 100Ω (Mode 2)
DRIVER: — MC 359 G

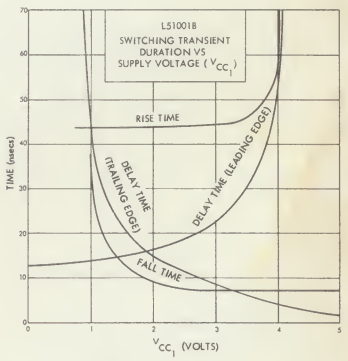
TEST CIRCUIT

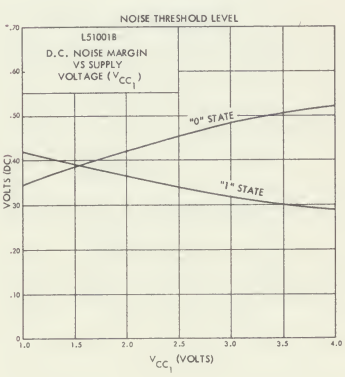


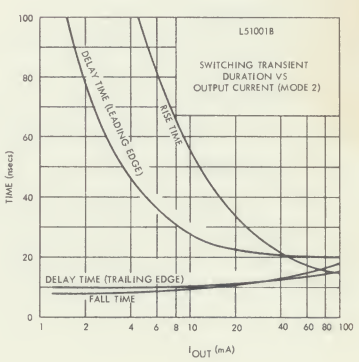
TYPICAL CHARACTERISTICS



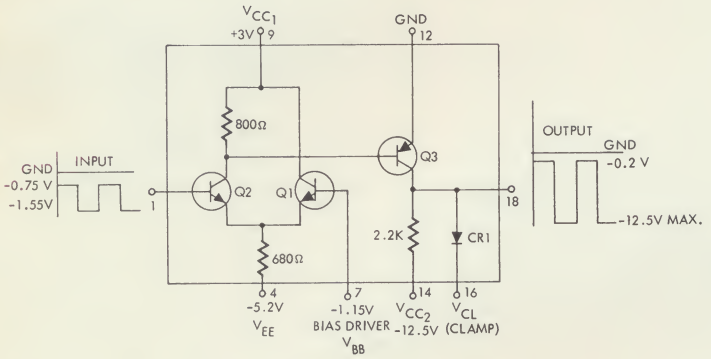


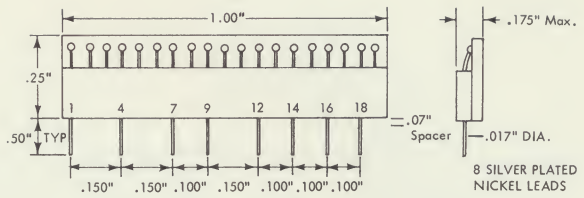






LEVEL ADJUSTORS — L51002B





OPERATIONAL CHARACTERISTICS

LOGIC STATE	INPUT LEVELS (VOLTS)	OUTPUT LEVELS (VOLTS)	POWER SUPPLY REQUIREMENTS (mA)				
			I_{IN}	I_{CC2}	I_{EE}	I_{BB}	I_{CC1}
"0"	−1.55	−6.0 to −12.5	0	0	4.5	.05	8.0
"1"	−0.75	−0.2	.04	5.6	5.5	0	6.0

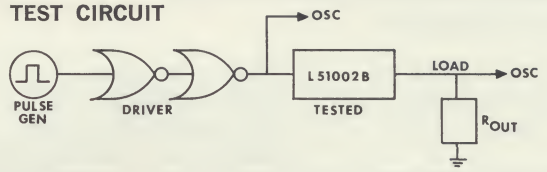
PARAMETER DERIVATION METHOD

TEST CONDITIONS

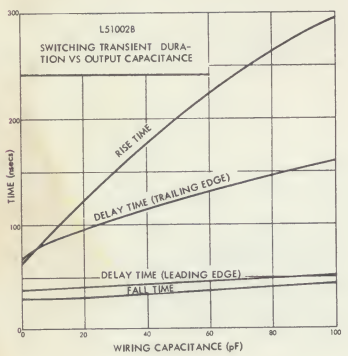
$V_{CC2} = -12.5V$ (or var)
$V_{EE} = -5.2V$
$V_{BB} = -1.15V$
$V_{CC1} = +3.0V$

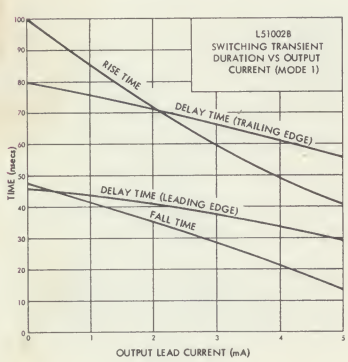
T amb = 25°C (or var)
R out = 2.2K (or var)
OSC: — Tektronix Type 585
DRIVER: — MC 359 G

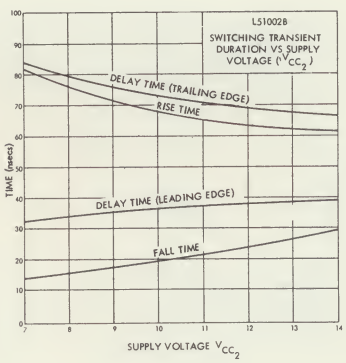
TEST CIRCUIT

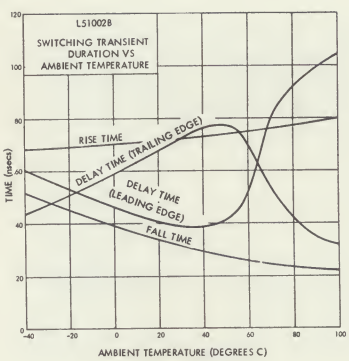


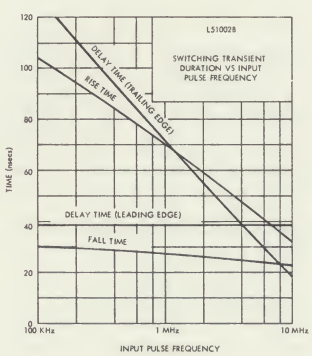
TYPICAL CHARACTERISTICS



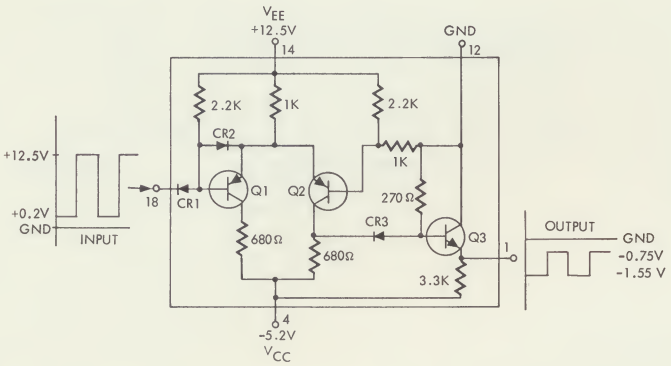


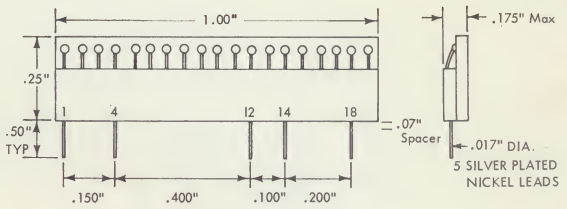






LEVEL ADJUSTOR — L51004A





OPERATIONAL CHARACTERISTICS

LOGIC STATE	INPUT LEVELS (VOLTS)	OUTPUT LEVELS (VOLTS)	POWER SUPPLY REQUIREMENTS (mA)			
			I_{IN}	I_{CC}	I_{EE}	I_{BB}
"0"	+0.2	−1.55	5.9	20.0	16.0	—
"1"	+6.0 to +12.5	−0.75	0	15.0	12.7	—

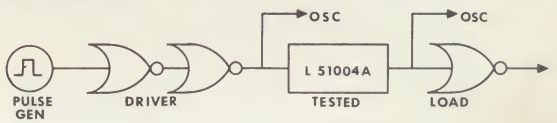
PARAMETER DERIVATION METHOD

TEST CONDITIONS

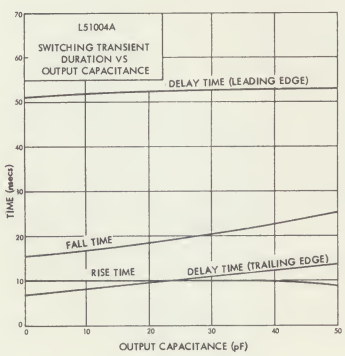
$V_{EE} = +12.5V$ (or var)
$V_{CC} = -5.2V$
$V_{BB} = -1.15V$

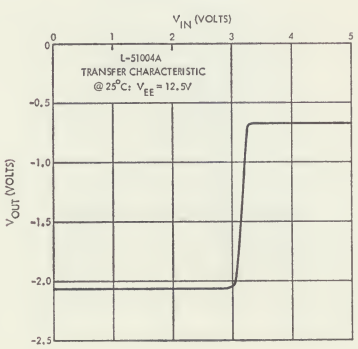
T amb = 25°C (or var)
LOAD: MC 359 G
OSC: Tektronix Type 585
DRIVER: INTELLUX GG 3515C

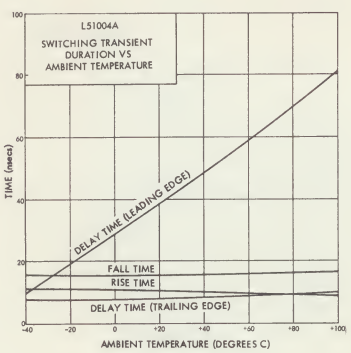
TEST CIRCUIT

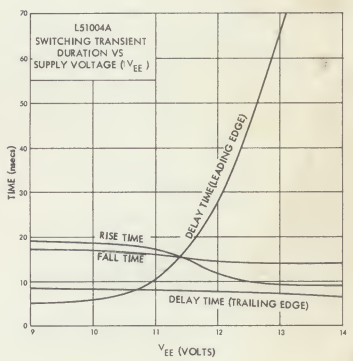


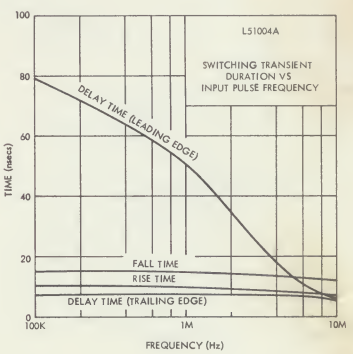
TYPICAL CHARACTERISTICS



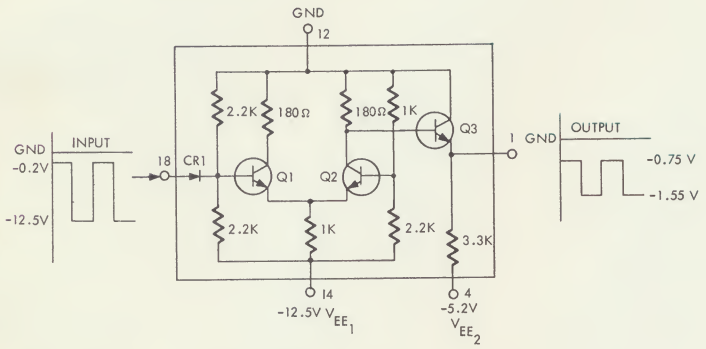


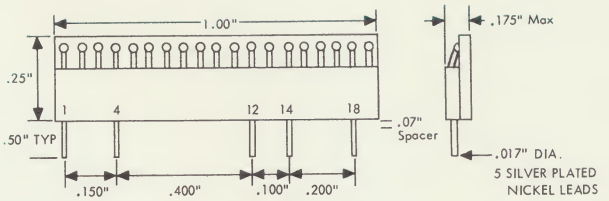






LEVEL ADJUSTOR — L51005A





OPERATIONAL CHARACTERISTICS

LOGIC STATE	INPUT LEVELS (VOLTS)	OUTPUT LEVELS (VOLTS)	POWER SUPPLY REQUIREMENTS (mA)			
			I_{IN}	I_{EE_1}	I_{EE_2}	I_{BB}
"0"	—6.0 to —12.5	—1.55	0	20.0	1.3	—
"1"	—0.2	—0.75	7.0	14.5	0.9	—

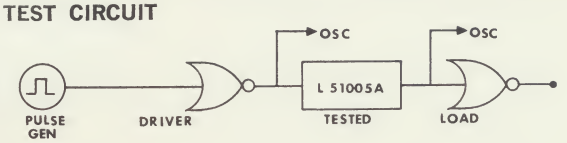
PARAMETER DERIVATION METHOD

TEST CONDITIONS

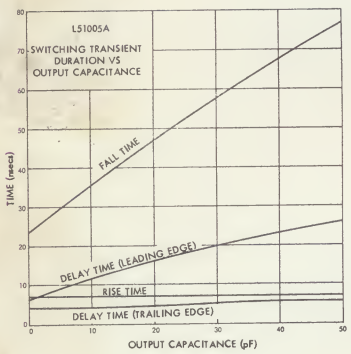
$V_{EE1} = -12.5V$ (or var)
$V_{EE2} = -5.2V$
$V_{BB} = -1.15V$

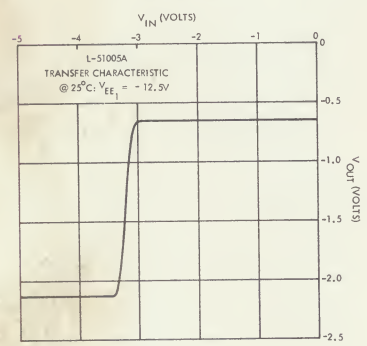
T amb = 25°C (or var)
LOAD = MC 359 G
OSC: Tektronix Type 585
DRIVER: 2N3250 (PNP)

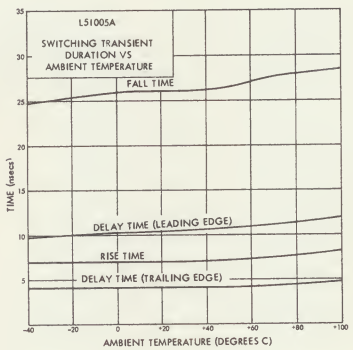
TEST CIRCUIT

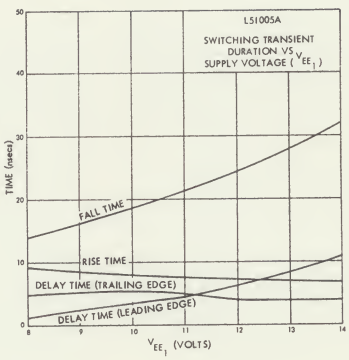


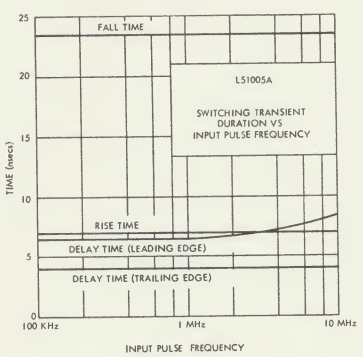
TYPICAL CHARACTERISTICS











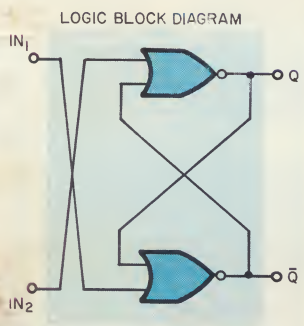
Treat the flip-flop logically. When you do, it becomes a simple matter to compare the different types and select the one that best fits your needs.

Your choice of a flip-flop depends on the function it is to perform and its compatibility with other logic elements in your system. So why not consider the flip-flop as a logic gating element for initial design purposes.

When considered as a logic-gating element, the flip-flop can be treated as a combination of two components—namely, a basic flip-flop and a steering circuit. The basic flip-flop is the memory element by virtue of its two stable states, while the steering circuit provides the input to the basic flip-flop, thus controlling its state.

Both the basic flip-flop and the steering circuit can be represented as a combination of two or more logic gates. On this basis, an analysis of the various types of flip-flops commonly used (R-S, J-K, etc.) can be made strictly from the standpoint of differences in their steering circuits.

A. C. Janecki, Senior Application Engineer, Intellux, Inc., Goleta, Cal.

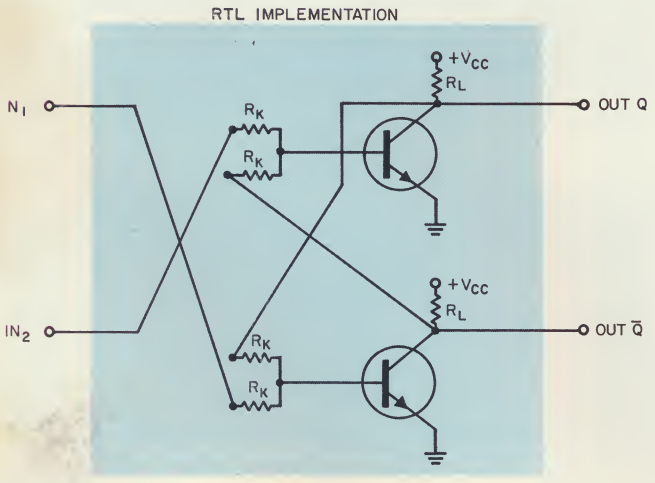


a

State table

IN 1	IN 2	Q_{t+1}	$\bar{Q}_{t+1}$
0	0	Q_t	$\bar{Q}_t$
0	1	0	1
1	0	1	0
1	1	0	0

b



c

1. **NOR-gate version** of the basic flip-flop is the most useful representation for positive-logic-system applications.

The basic flip-flop

The basic flip-flop can be obtained by cross-connecting two transistorized gates so that each forms a feedback loop for the other. Four different configurations are possible, since AND, OR, NAND or NOR gates can be used. Although all four configurations are equally useful as logic representations of the basic flip-flop, there is usually one that is most appropriate for a specific application.

The NOR-gate (Fig. 1a) is the most suitable to use in a positive-logic system, because the "no-change" condition of the flip-flop occurs for the low (logic "0") state of both inputs (Fig. 1b). The following analysis of flip-flop types is arbitrarily limited to positive-logic systems, so the NOR-gate version of the basic flip-flop will be used exclusively.

The RTL circuit implementation of the NOR-gate flip-flop is shown in Fig. 1c. Each input terminal is placed in line with the output terminal it controls. Thus, Output Q will become high (logic "1") when Input "1" is high, etc.

The R-S flip-flop

The steering circuit for the R-S flip-flop (Fig. 2) is simply two OR gates. They are used to "set" and "clear" (reset) the flip-flop in applications where there is no possibility of both inputs being high (or "1") at the same time. If only one "set" input and one "clear" input to the gates are used, the R-S flip-flop becomes identical with the basic flip-flop.

The logic state table of the R-S flip-flop shows the logic states of the two outputs (called Q_{t+1} and $\bar{Q}_{t+1}$) at some period $t+1$. These outputs are due to the logic states of the two inputs S_{t+1} and C_{t+1} at the same period $t+1$.

In this flip-flop, a knowledge of the logic states of the two inputs during the previous period "t" is not necessary. Only the input states at $t+1$ are needed to determine Q_{t+1} and $\bar{Q}_{t+1}$. For example, when both inputs are "0" at $t+1$, the two outputs at $t+1$ will remain the same as they were at t (Fig. 2b). Similarly, for $S_{t+1} = 0$ and $C_{t+1} = 1$,

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the outputs will become $Q_{t+1} = 0$, and $\bar{Q}_{t+1} = 1$ independently of the states Q_t and $\bar{Q}_t$ in the previous period t.

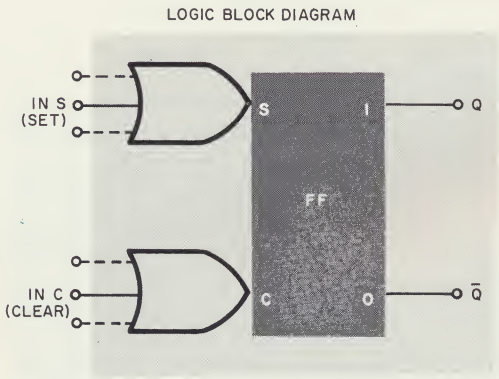
The gated flip-flop

If there is the possibility that both the "set" and "clear" inputs to a flip-flop can be high at the same time, suitable gating must be used in the steering circuit to prevent both outputs from becoming "0." Such a circuit, consisting of two AND gates, is shown in Fig. 3.

In this scheme, only the gate connected to the high output of the flip-flop is enabled. The other gate is simultaneously inhibited by the low output. Only one of the two incoming signals can reach the flip-flop at any one time, so both outputs cannot assume the same state. However, if both input lines are made high simultaneously, another problem arises: The circuit will oscillate, since the two AND gates will be alternately enabled by the flip-flop outputs. The frequency of this oscillation depends on the propagation-delay times of the gates and the basic flip-flop in series.

To prevent oscillation, the input signals should be removed from the gates before the flip-flop outputs complete the change-over. In other words, the input signals should be shorter than the combined propagation delay time of the circuit. Such short pulses will switch the flip-flop to its complement state without causing oscillation.

These short pulses, or spikes, are called ac



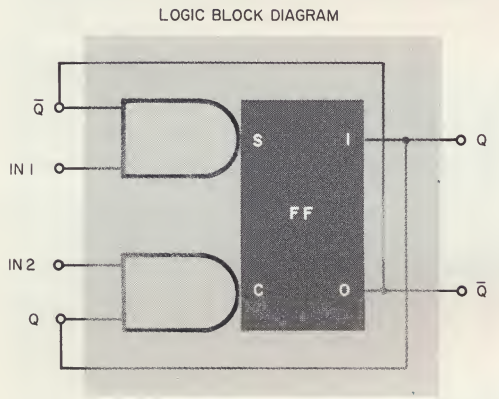
a

State table

States of inputs at t+1		Resulting states of outputs at t+1		
S_{t+1}	C_{t+1}	Q_{t+1}	$\bar{Q}_{t+1}$	Comments
0	0	Q_t	$\bar{Q}_t$	No change from previous state
0	1	0	1	Independent of previous state
1	0	1	0	Independent of previous state
1	1	0	0	Not permitted

b

2. **R-S flip-flop** has the simplest form of a steering circuit: just two OR gates.



a

State table for dc inputs

States of inputs at t+1		Resulting states of outputs at t+1		
$(IN\ 1)_{t+1}$	$(IN\ 2)_{t+1}$	Q_{t+1}	$\bar{Q}_{t+1}$	Comments
0	0	Q_t	$\bar{Q}_t$	No change from previous state
0	1	0	1	Independent of previous state
1	0	1	0	Independent of previous state
1	1	~	~	Oscillating

b

State table for ac inputs

States of inputs at t+1		Resulting states of outputs at t+1		
$(IN\ 1)_{t+1}$	$(IN\ 2)_{t+1}$	Q_{t+1}	$\bar{Q}_{t+1}$	Comments
0	0	Q_t	$\bar{Q}_t$	No change from previous state
0	1	0	1	Independent of previous state
1	0	1	0	Independent of previous state
1	1	$\bar{Q}_t$	Q_t	Change to complement state

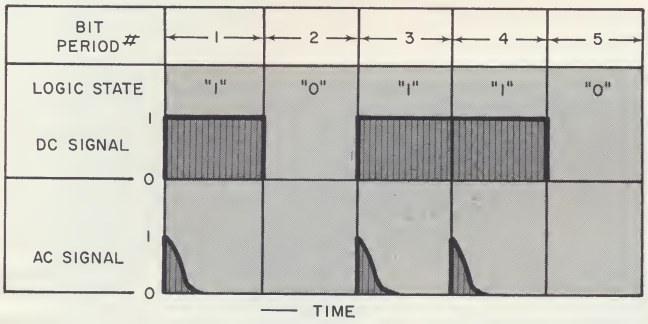
c

3. **Gated flip-flop** has a steering circ... that prevents both flip-flop outputs f... becoming "0" at the same time. Ac... input pulses must be used to prevent the flip-flop from oscillating. This situation can arise if both input lines are made high simultaneously.

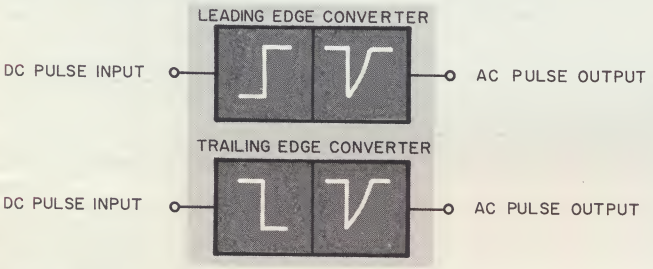
pulses and can be located anywhere within the bit period of the input signal. Usually, they are located either at the very beginning or at the very end of the period (Fig. 4).

The J-K flip-flop

The input pulses to a gated flip-flop must be narrow enough to prevent oscillation, and they must at the same time have enough energy to cause reliable triggering of the flip-flop. This would indicate the need for a special input device that is matched to the requirements of the particular flip-flop. Such a device forms a part of the steering circuit and allows the flip-flop to be operated from dc signals of various widths without causing oscillations. The resulting circuit is called a J-K flip-flop.



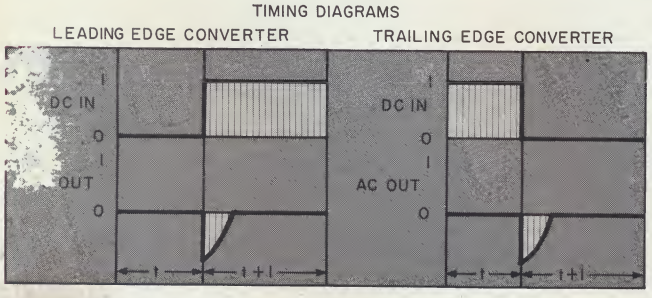
4. **Ac input pulses** usually coincide with either the beginning or the end of the bit period.



State table

dc IN $_t$	dc IN $_{t+1}$	ac OUT $_{t+1}$	
		Leading edge converter	Trailing edge converter
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	0

ⓐ



ⓑ

5. **Dc-to-ac pulse conversion** can be either the leading-edge or trailing-edge type. The state tables relating the logical states of the input and output pulses are different for each type.

The input device is, in effect, a dc-to-ac pulse converter. The conversion may be obtained by passing the incoming pulse through a delay element in parallel with the gate and using the delayed pulse to inhibit the gate. A short pulse will thus appear at the output of the gate, its width equal to the delay time of the delay element.

A more straightforward method is to pass the dc signal through a differentiating circuit, and use the output spike as the ac pulse. This type of device will be considered here.

With the differentiating-type converter, the output ac pulse can be obtained either at the leading edge or trailing edge of the dc input pulse. Since the output pulse is produced by the change in the voltage levels, both the voltage level (logic state) in the initial period t and the voltage level in the succeeding period $t + 1$ must be known to determine whether an output pulse will occur in period $t + 1$ (Fig. 5). This differs from the R-S flip-flop, in which only the states of the inputs at period $t + 1$ are significant. The trailing-edge triggering is usually preferred in positive-logic systems because it prevents false operation in multi-input flip-flop applications.

Fig. 6 shows the complete J-K flip-flop that can be operated by dc input pulses. The signal-flow diagram (Fig. 6a) illustrates the principle of pulse conversion, from dc to ac and back to dc, employed in this flip-flop. Fig. 6c shows the complete table of logic states, assuming dc pulses at the J and K inputs. This table is derived from the table of logic states shown in Fig. 3c, with the addition, however, of the converter logic (Fig. 5a).

There are three logic functions that have to be implemented in the J-K flip-flop. They are the dc-to-ac pulse conversion, the AND gating and the memory function (basic flip-flop). The dc/ac conversion is achieved most conveniently by a simple RC differentiating circuit. In this circuit, however, the desirable trailing-edge pulse is negative. The pulse must therefore be inverted before being fed into the AND gate.

A more economical approach is to use a complementary AND gate that will process the original negative pulse without the necessity for inversion. Now, however, the enabling dc signals from the outputs of the flip-flop must be inverted. This can easily be done by switching the connections of the complementary outputs, which by definition are the inverse of each other. The modified logic-block diagram is shown in Fig. 7a.

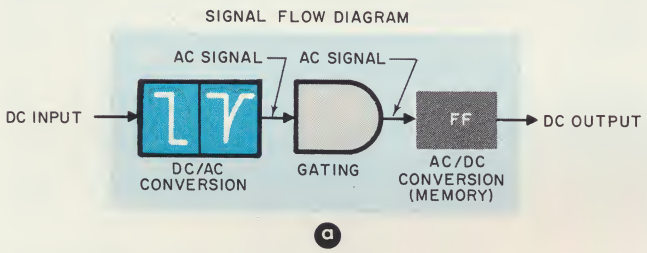
Fig. 7b shows the RTL circuit implementation of the J-K flip-flop. The dc/ac pulse converter is equipped with a diode, CR, which transmits the negative trailing-edge pulse and blocks the positive leading-edge pulse. The complementary AND gate is of the resistive Kirchhoff type, which will pass the negative pulse to the transistor base when enabled by a low signal from one of the flip-

flop outputs. The connections from the gates to the transistors are reversed because of the negative pulse, which must de-saturate the ON transistor, instead of saturating the OFF transistor, as in positive-pulse applications.

Fig. 7c shows the familiar re-organized schematic of the J-K flip-flop. Resistors R_c' and R_c'' are combined into one resistor, R_c, because point a of R_c' should logically be at the same level as the output Q of the flip-flop, and diode CR is relocated toward the base. Thus, R_c' and R_c'' are in parallel and can be replaced with one resistor. The same situation holds for resistors R_k' and R_k''. As a result, these two can also be replaced with a single resistor—namely, R_k.

The T flip-flop

It can be seen from the state table in Fig. 6c that when both the dc inputs to a J-K flip-flop change simultaneously from "1" to "0," the flip-flop changes states for any initial conditions of the outputs. This property is utilized in the so-called T (for toggle or trigger) flip-flop, where the two input lines are connected together into only one input (Fig. 8a).



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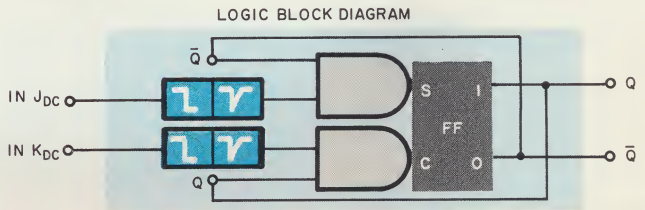


b

State table

States of inputs at t		States of inputs at t+1			Resulting states of outputs at t+1	
J_t	K_t	J_{t+1}	K_{t+1}	Q_{t+1}	$\bar{Q}_{t+1}$	Comments
0	0	0	0	Q_t	$\bar{Q}_t$	No change from previous state
0	0	0	1	Q_t	$\bar{Q}_t$	
0	0	1	0	Q_t	$\bar{Q}_t$	
0	0	1	1	Q_t	$\bar{Q}_t$	
0	1	0	0	0	1	Independent of previous state
0	1	0	1	Q_t	$\bar{Q}_t$	No change from previous state
0	1	1	0	0	1	Independent of previous state
0	1	1	1	Q_t	$\bar{Q}_t$	No change from previous state
1	0	0	0	1	0	Independent of previous state
1	0	0	1	1	0	
1	0	1	0	Q_t	$\bar{Q}_t$	No change from previous state
1	0	1	1	Q_t	$\bar{Q}_t$	
1	1	0	0	$\bar{Q}_t$	Q_t	Change to complement state
1	1	0	1	1	0	Independent of previous state
1	1	1	0	0	1	
1	1	1	1	Q_t	$\bar{Q}_t$	No change from previous state

c

6. **J-K flip-flop** is a gated flip-flop than can be operated by dc input pulses.

In this type of flip-flop, sometimes also referred to as a "binary," the outputs change state each time the input-signal voltage falls from "1" to "0," and remain unchanged when the input-signal voltage rises from "0" to "1." Thus, there is one change in output state for every two changes in input signal. This means that the frequency of the output is half the frequency of the input. A variety of frequency dividers and counters can be built utilizing this property.

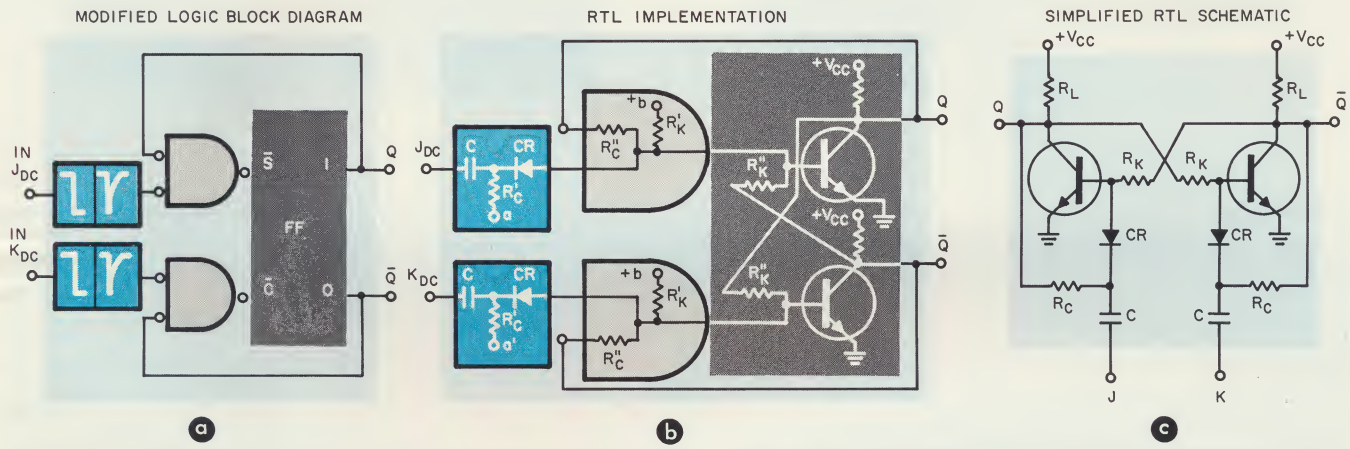
The toggle flip-flop can be implemented by exactly the same circuit as the J-K flip-flop. The two input terminals, J and K, are simply connected together to form the T terminal (Fig. 8b).

The delay flip-flop

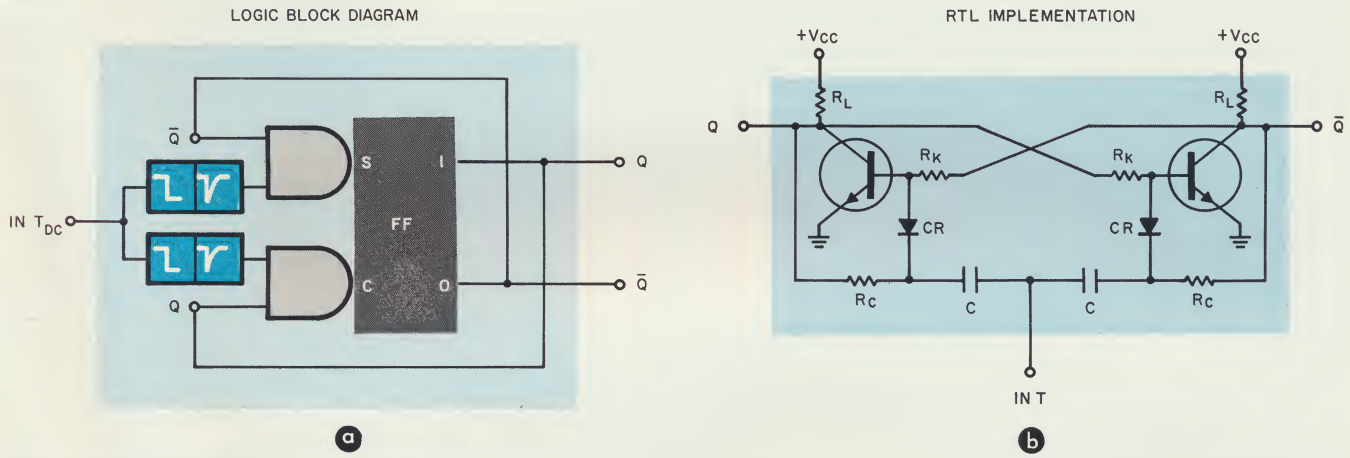
In the T flip-flop (Fig. 8a), one of the inputs to each AND gate either enables or inhibits the gate. For reliable operation of the flip-flop, these Q and $\overline{Q}$ steering signals should reach the gate a certain time before the triggering signal, T, to ensure that the gates are fully enabled.

The enabling terminals of the flip-flop can be connected to some other points in the system, instead of to the Q and $\overline{Q}$ outputs used in the T

(continued on pg 55)



7. **Practical J-K flip-flop** accomplishes ac/dc conversion by RC differentiation. Complementary AND gates are used at the inputs, and the input connections to these gates from the flip-flop outputs are reversed.



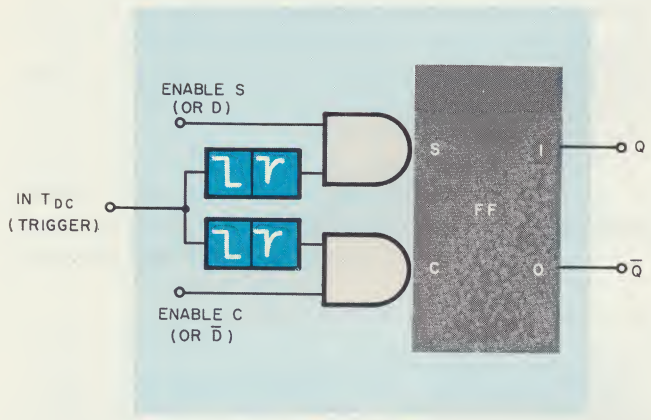
State table (trailing-edge converter)

State of input at t	State of input at t+1	Resulting states of outputs at t+1		
T_t	T_{t+1}	Q_{t+1}	$\overline{Q}_{t+1}$	Comments
0	0	Q_t	$\overline{Q}_t$	No change from previous state
0	1	Q_t	$\overline{Q}_t$	No change from previous state
1	0	$\overline{Q}_t$	Q_t	Change to complement state
1	1	Q_t	$\overline{Q}_t$	No change from previous state

c

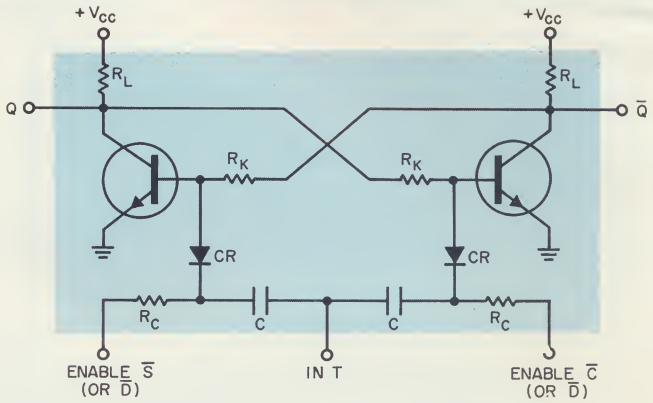
8. **T flip-flop** is the same as the J-K flip-flop, except that it has a single input formed by connecting J and K.

LOGIC BLOCK DIAGRAM



a

RTL IMPLEMENTATION



b

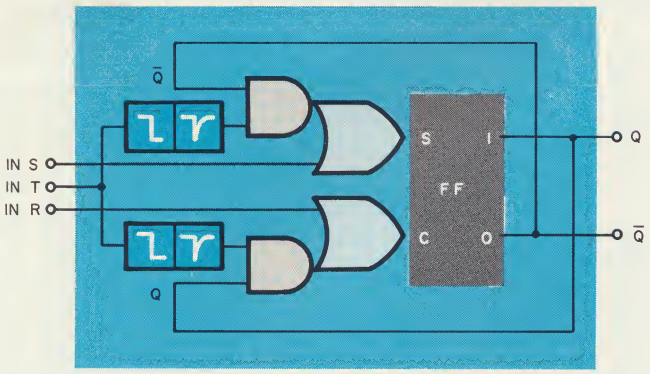
State table

State of inputs at t			State of input at t+1	Resulting states of outputs at t+1		
S_t or D_t	C_t or $\bar{D}_t$	T_t	T_{t+1}	Q_{t+1}	$\bar{Q}_{t+1}$	Comments
0	0	0	0	Q_t	$\bar{Q}_t$	No change from previous state
0	0	0	1	Q_t	$\bar{Q}_t$	
0	0	1	0	Q_t	$\bar{Q}_t$	
0	0	1	1	Q_t	$\bar{Q}_t$	
0	1	0	0	Q_t	$\bar{Q}_t$	
0	1	0	1	Q_t	$\bar{Q}_t$	
0	1	1	0	0	1	$Q_{t+1}=S_t$; $\bar{Q}_{t+1}=C_t$
0	1	1	1	Q_t	$\bar{Q}_t$	No change from previous state
1	0	0	0	Q_t	$\bar{Q}_t$	
1	0	0	1	Q_t	$\bar{Q}_t$	
1	0	1	0	1	0	$Q_{t+1}=S_t$; $\bar{Q}_{t+1}=C_t$
1	0	1	1	Q_t	$\bar{Q}_t$	
1	1	0	0	Q_t	$\bar{Q}_t$	No change from previous state
1	1	0	1	Q_t	$\bar{Q}_t$	
1	1	1	0	?	?	Indeterminate
1	1	1	1	Q_t	$\bar{Q}_t$	No change from previous state

c

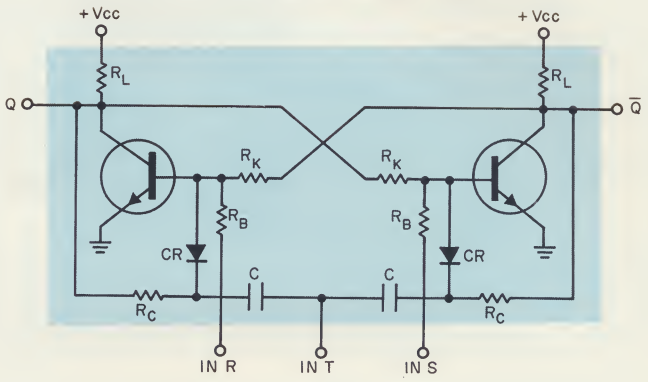
9. **Delay flip-flop** has its enabling signals applied from some point external to the basic flip-flop. Its state table (c) can be reduced to that portion shown in white if the inputs are complementary.

LOGIC BLOCK DIAGRAM



(a)

RTL IMPLEMENTATION



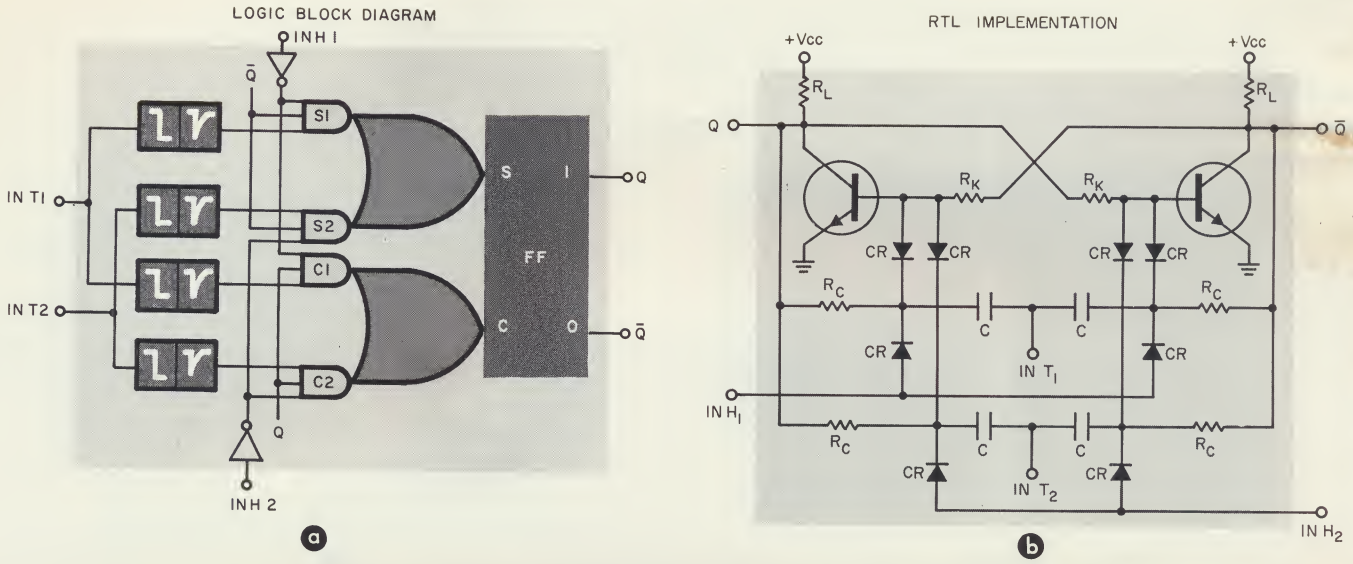
(b)

State table (trailing-edge converter)

State of inputs at t			State of inputs at t+1	Resulting states of outputs at t+1		
S_t	R_t	T_t	T_{t+1}	Q_{t+1}	$\bar{Q}_{t+1}$	Comments
0	0	0	0	Q_t	$\bar{Q}_t$	No change from previous state
0	0	0	1	Q_t	$\bar{Q}_t$	
0	0	1	0	$\bar{Q}_t$	Q_t	Change to complement state
0	0	1	1	Q_t	$\bar{Q}_t$	No change from previous state
0	1	0	0	0	1	Independent of previous state
0	1	0	1	0	1	
0	1	1	0	?	?	Indeterminate
0	1	1	1	0	1	Independent of previous state
1	0	0	0	1	0	
1	0	0	1	1	0	
1	0	1	0	?	?	Indeterminate
1	0	1	1	1	0	Independent of previous state
1	1	0	0	0	0	Not permitted
1	1	0	1	0	0	
1	1	1	0	0	0	
1	1	1	1	0	0	

(c)

10. **R-S-T flip-flop** incorporates the steering circuits of both the R-S and T flip-flops.



11. **Up-down flip-flop** has both "toggle" inputs and "inhibit" inputs.

flip-flop. This type of steering circuit characterizes the so-called "delay" flip-flop, (Fig. 9a).

Here the triggering signal, T, is coupled through the dc/ac converters, and the two enabling signals S and C are dc-coupled to the flip-flop. For correct operation, signals S and C should be established in period t, before the arrival of the ac-pulse T in period $t + 1$. Therefore, signals S and C are assumed to be the same in both t and $t+1$ periods. Only the dc input T may change its state from T_t to T_{t+1}, causing, under appropriate conditions, the appearance of the ac pulse T_{ac} at $t + 1$.

The ac pulse T_{ac} acts as a searching, or sampling, signal, in that it detects the states of the S and C inputs and transfers them to the outputs of the flip-flop. In this way, the outputs of the flip-flop in period $t+1$ will become the same as the inputs S and C were in the previous t period. Hence, the name "delay" flip-flop. The state table of the delay flip-flop is shown on Fig. 9c.

The two input signals S and C are usually complementary. When this is the case, the designations of the input terminals are D and $\overline{D}$, and the state table of the delay flip-flop can be simplified to that shown on the white portion of Fig. 9c.

The RTL implementation of the delay flip-flop (Fig. 9b) is again the same as the T flip-flop, except that the enabling inputs to the two AND gates are disconnected from the flip-flop outputs and are available for external connections.

The R-S-T flip-flop

Another very useful type of steering circuit is used in the so-called R-S-T flip-flop, shown with its state table in Fig. 10. It is an ORed combination of the R-S and the T steering circuits and can serve as any one of them, as required. It is used mostly as a "presettable" and "clearable" toggle flip-flop in binary counters.

The implementation of the R-S-T flip-flop (Fig. 10b) is basically the same as that of the T flip-flop. The only difference is the addition of the two resistors, R_B, for dc coupling inputs R and S to the circuit.

The up-down flip-flop

All the input terminals of a steering circuit that serve to enable the flip-flop when a positive dc signal is applied to them (in positive-logic systems) are called the "enabling inputs," or simply "inputs" (*IN.S*, *IN.C*, etc.) Similarly, the terminals that serve to prevent (inhibit) the switching of the flip-flop on a positive signal are called "inhibiting inputs" (*INH.S*, *INH.C*, etc.).

A toggle flip-flop equipped with two sets of T inputs and two sets of inhibiting inputs is shown in Fig. 11. This is the "up-down flip-flop" used in reversible counters and similar devices. When *INH.*1 is high, gates S_1 and C_1 are inhibited, and only signals applied to $IN.T_2$ will operate the flip-flop. Changing *INH.1* to low and *INH.2* to high will activate the signal applied to $IN.T_1$ instead. The state table of this flip-flop is similar to the combination of two state tables of a T flip-flop, one for the *INH.1* input when high, and the other for the *INH.2* input when high. ■ ■

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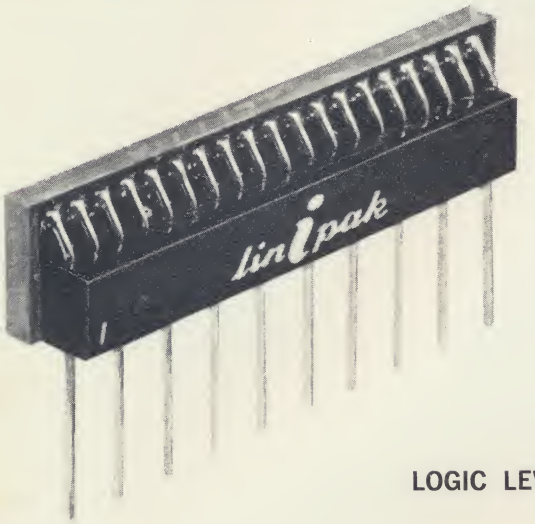

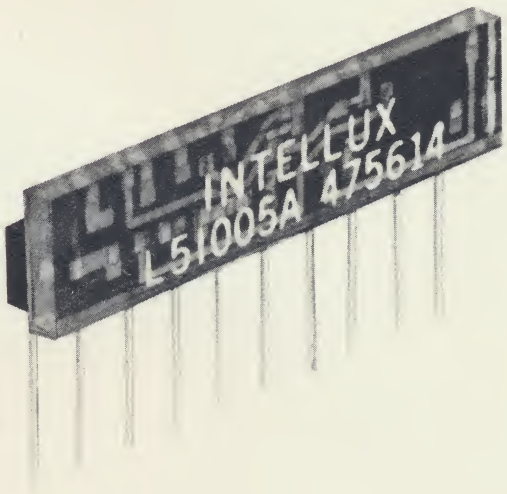

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